CLAIMS

What is claimed is:

1. A method of increasing voltage available to a memory element, comprising:

providing a current in a plurality of memory write lines, wherein the write lines are magnetically coupled to at least one memory element;

coupling a first and second plurality of transistors to either end of the memory write line; and

altering the conduction state of individual transistors within the first and second plurality of transistors.

2. The method of claim 1, wherein the amount of voltage available to the memory element is increased.

3. The method of claim 1, wherein the individual transistors within the first and second pluralities of transistors are coupled in parallel and are binary weighted.

4. The method of claim 1, wherein the amount of voltage available may be controlled by modifying the conduction state of the first and second plurality of transistors.

5. The method of claim 1, further comprising coupling a power supply to the first and second plurality of transistors, wherein the power supply has approximately constant voltage and provides a variable current.

6. A memory, comprising:

a plurality of memory write lines magnetically coupled to at least one magnetic memory element;

a write circuit including a plurality of transistors that are coupled to a memory write line;

wherein individual transistors within the plurality of transistors are in parallel and may have their conduction states modified independent of each other; and

whereby the amount of voltage available to the memory element is increased.

7. The memory of claim 6, further comprising logic coupled to the plurality of transistors, wherein the logic modifies the conduction state of individual transistors.

8. The memory of claim 7, wherein the individual transistors within the plurality of transistors are binary weighted.

9. The memory of claim 6, further comprising a first and second plurality of transistors, wherein the first plurality of transistors source current in the memory write lines and the second plurality of transistors sink current from the memory write lines.

10. The memory of claim 9, wherein the first plurality of transistors comprise p-channel metal oxide semiconductor field effect transistors ("MOSFETs"), and the second plurality of transistors comprise n-channel MOSFETs.

11. The memory of claim 6, wherein the logic is coupled to the gate terminals of the plurality of transistors.

12. The memory of claim 6, wherein the amount of current in the write line may be controlled by modifying the conduction state of individual transistors within the plurality of transistors.

13. The memory of claim 6, further comprising a power supply coupled to the write circuit, wherein the power supply has approximately constant voltage and provides a variable current.

14. A memory, comprising:

at least one memory write line that is magnetically coupled to at least one magnetic memory element;

a write circuit including first and second transistors that are coupled to either end of the memory write line;

wherein the conduction state of the first transistor is controlled by an inverter circuit;

wherein the inverter circuit electrically couples a write signal to the first transistor; and

whereby the amount of voltage provided to the memory element is increased.

15. The memory of claim 14, wherein the conduction state of the first transistor is varied as the write signal is varied.

16. The memory of claim 15, wherein a control signal is coupled to the input of the inverter and controls the conduction state of the inverter.

17. The memory of claim 14, wherein the threshold voltage for the inverter is varied as the write signal is varied.

18. The memory of claim 14, further comprising a power supply coupled to the write circuit, wherein the power supply has approximately constant voltage and provides a variable current.

19. The memory of claim 14, wherein the first transistor sources current to the memory write line and the second transistor sinks current from the memory write line.

20. A circuit for controlling current to a magnetic memory array, comprising:

providing means for providing current to a conductor;

sinking means for sinking current from the conductor;

wherein said conductor is magnetically coupled to coupled to a magnetic memory element.

21. The circuit of claim 20, further comprising a controlling means for controlling the conduction state of said providing means and said sinking means.

22. The circuit of claim 21, wherein altering said conduction state results in altering the digital state of the magnetic memory element.

23. The circuit of claim 20, further comprising means for supplying power to the circuit.

24. The circuit of claim 23, wherein the means for supplying power has approximately constant voltage and provides a variable current.

25. A computer system, comprising:

a processor;

a bridge logic device coupled to the processor; and

a system memory coupled to said processor, wherein the system memory includes:

a power supply;

a first transistor coupled to the power supply;

a write conductor coupled to the first transistor, wherein the write conductor is magnetically coupled to a magnetic memory element;

a second transistor coupled to the write conductor, ground, and the power supply;

an inverter coupled the first transistor, wherein the inverter controls the conduction state of the first transistor;

wherein the power supply has approximately constant voltage and provide a variable current; and

wherein the amount of voltage drawn from the power supply is minimized.

26. The computer system of claim 25, wherein a control signal is coupled to the input of the inverter and controls the conduction state of the inverter.

27. The computer system of claim 25, wherein the threshold voltage for the inverter is variable.

28. The computer system of claim 25, wherein the first transistor sources current to the memory write line and the second transistor sinks current from the memory write line.